REMARKS/ARGUMENTS

The present amendment is in response to the Office Action mailed December 31, 2002, in which Claims 1 through 20 were rejected. Applicant has thoroughly reviewed the outstanding Office Action including the Examiner's remarks and the reference cited therein. The following remarks are believed to be fully responsive to the Office Action and, when coupled with the amendments made herein, are believed to render all claims at issue patentably distinguishable over the cited references.

Claims 6, 8 and 16 are amended herein. Claims 1 through 5, 7 and 11 through 15 are cancelled. No claims are added. Accordingly, Claims 6, 8, 9, 10, and 16 through 20 remain pending.

All the changes are made for clarification and are based on the application and drawings as originally filed. It is respectfully submitted that no new matter is added.

Applicant respectfully requests reconsideration in light of the above amendments and the following remarks.

CLAIM REJECTIONS – 35 U.S.C. SECTION 103(a)

1. Claims 1 and 5

With respect to Paragraphs 1 and 2 of the final Office Action, the Examiner rejected Claims 1 and 5 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,933,733 to Feria et al. (hereinafter referred to as "Feria et al.") in view of U.S. Patent No. 5,972,783 to Arai et al. (hereinafter referred to as "Arai et al."). Of the rejected claims, Claim 1 is independent.

Claims 1 and 5 are cancelled herein, thus rendering this rejection moot. Applicant respectfully requests that the Examiner's 35 U.S.C. 103 (a) rejection of Claims 1 and 5 be reconsidered and withdrawn.

2. Claims 2 through 4

With respect to Paragraphs 1 and 3 of the final Office Action, the Examiner rejected Claims 2 through 4 under 35 U.S.C. 103(a) as being unpatentable over Feria et al. in view of Arai et al. and in further view of U.S. Patent No. 4,937,756 to Hsu et al. (hereinafter referred to as "Hsu et al.")

Claims 2 through 4 are cancelled herein, thus rendering this rejection moot. Applicant respectfully requests that the Examiner's 35 U.S.C. 103 (a) rejection of Claims 2 through 4 be reconsidered and withdrawn.

3. Claims 6, 9, 10, 11, 14 and 15

With respect to Paragraphs 1 and 4 of the final Office Action, the Examiner rejected Claims 6, 9, 10, 11, 14 and 15 under 35 U.S.C. 103(a) as being unpatentable over Feria et al. in view of Arai et al. and in further view of U.S. Patent No. 6,030,871 (Eitan). Claims 6 and 11 are independent claims.

Applicant respectfully traverses this rejection.

Claims 7 and 11 through 15 have been cancelled, thus rendering this aspect of the rejection moot.

Claims 6 and 8 are amended herein. Amended Claim 6 recites forming a stacked oxide-nitride-oxide layer on a P-type semiconductor substrate, patterning the stacked oxide-nitride-oxide layer to form a plurality of nitride read only memory cells on the P-type semiconductor substrate, and forming a plurality of indium pocket regions in the P-type semiconductor substrate under the gate structure of each of the nitride read only memory cells, and afterward, performing an N-type ion implantation to form a plurality of N-type ion-implanted regions in the P-type semiconductor substrate beside each of the indium pocket regions.

With regard to the cited reference, Feria et al., this reference teaches a process to form memory cells wherein a P-type semiconductor substrate is provided (see col. 8, lines 15-25), and a dielectric layer is formed thereon (see FIG. 2). On the dielectric layer a photoresistor layer is formed and patterned to expose a portion of the dielectric layer (see FIG. 3). The dielectric layer is then etched using the photoresistor layer as a mask (see FIG. 3). Then, an N-type

ion implantation is performed to form a plurality of N-type ion-implanting regions in the P-type semiconductor substrate so as to form source/drain regions (see FIG. 4). Afterward, an ion implantation is performed to form a plurality of pocket dopant regions each of which beside one of source/drain regions (see FIGs. 5-6).

With regard to the cited reference, Arai et al., this reference teaches a process for producing MOS transistors wherein an ion implantation step to form pockets comprises the implantation of indium (see col. 20, lines 15-20).

With regard to the cited reference, Eitan et al., this reference teaches the formation of memory cells, wherein a sacrificial oxide layer is formed on the semiconductor substrate, then a first ion implantation is performed to form source/drain regions and a second ion implantation is performed to form pocket dopant regions (see FIG. 4A to FIG. 4C).

As claimed in amended Claim 6, the stacked oxide-nitride-oxide is formed on the P-type semiconductor substrate prior to the indium pocket regions and the source/drain regions, which can prevent undesired diffusion of the implanted dopants caused by later thermal steps of forming the gate insulating layer of stacked oxide-nitride-oxide. However, all of the three cited references, Feria et al., Arai et al. and Eitan et al. fail to teach or suggest forming a stacked oxide-nitride-oxide layer on the semiconductor substrate before the ion implantation steps. Thus, it is not obvious for one-skilled in the art to deduce amended Claim 6 in view of Feria et al., Arai et al. and Eitan et al. Applicant respectfully submits that amended Claim 6 is patentably distinguishable over the three cited references.

Amended Claim 8 and Claims 9 and 10 depend upon Claim 6, each of which including all limitations thereof. Thus, amended Claim 8 and Claims 9 and 10 are also patentably distinguishable over the three cited references.

Applicant respectfully requests that the Examiner's 35 U.S.C. 103(a) rejection of Claims 6, 9, 10, 11, 14 and 15 be reconsidered and withdrawn.

4. Claims 7, 8, 12, 13 and 16 through 20

With respect to Paragraphs 1 and 5 of the final Office Action, the Examiner rejected Claims 7, 8, 12, 13 and 16 through 20 under 35 U.S.C. 103(a) as being unpatentable over Feria et al. in view of Arai et al. and Eitan and in further view of Hsu et al. Claim 16 is an independent claim.

Applicant respectfully traverses this rejection.

Amended Claim 16 recites forming a stacked oxide-nitride-oxide layer on a P-type semiconductor substrate, patterning the stacked oxide-nitride-oxide layer to form a plurality of nitride read only memory cells on the P-type semiconductor substrate, and performing an N-type ion implantation to form a plurality of N-type ion-implanted regions in the P-type semiconductor substrate to form source/drain regions, then forming a plurality of indium pocket regions in the P-type semiconductor substrate, each of which beside one of the source/drain regions.

With regard to the cited reference, Hsu et al., see col. 3, lines 30-45 and FIG. 4-4, which teaches that a certain amount of boron is implanted into the isolation region as shown by numeral 4 before the GIS is defined. And a composite thermal oxide-nitride-oxide structure is formed on the P-type

semiconductor substrate as the GIS gate insulator 5.

It is apparent that Hsu et al. fail to teach or suggest forming a stacked oxide-nitride-oxide layer on the semiconductor substrate before the ion implantation step. Thus, it is not obvious for one-skilled in the art to deduce amended Claim 16 in view of Feria et al., Arai et al., Eitan et al. and Hsu et al. Applicant respectfully submits that amended Claim 16 is patentably distinguishable over the four cited references.

Claims 17 through 20 depend upon Claim 16, each of which includes all limitations thereof. Thus, it is respectfully submitted that Claims 17 through 20 are also distinguishable over the four cited references.

Amended Claim 8 is also patentably distinguishable over the four cited references based on the same reason.

Applicant respectfully requests that the Examiner's 35 U.S.C. 103(a) rejection of Claims 7, 8, 12, 13 and 16-20 be reconsidered and withdrawn.

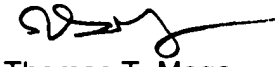
CONCLUSION

In light of the above amendments and remarks, Applicants respectfully submit that all pending claims as currently presented are in condition for allowance. If, for any reason, the Examiner disagrees, please call the undersigned attorney at 202-624-3947 in an effort to resolve any matter still outstanding *before* issuing another action. The undersigned attorney is confident that any issue which might remain can readily be worked

out by telephone.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,



Thomas T. Moga
Registration No. 34,881
Attorney for Applicant

DICKINSON WRIGHT PLLC
1901 L Street, N.W., Suite 800
Washington, D.C. 20036
202-457-0160

Dated: **August 21, 2003**

TTM/hs